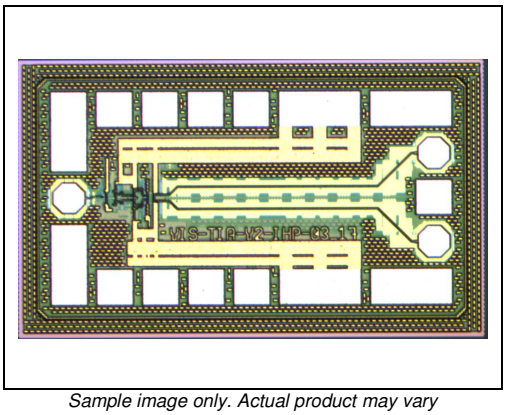
Datasheet

T56-250v1

Vertically Integrated Systems

Transimpedance Amplifier 56 Gbit/s



Sample image only. Actual product may vary

Product Code: T56-250v1

Preliminary

Product Description

The T56-250C is a high speed transimpedance amplifier (TIA) IC designed for use by 56G receiver modules in fiber optic transmission systems. The T56-250 operates from a single +3.3 V supply typically dissipating 250 mW of DC power and is designed for the use with PIN photodetectors in a wire-bond assembly

The IC has a single-ended input (IN) and a differential output (OutP, OutN). It includes the cathode connection for the photodiode (Cath) as well as a bias path through the internal pin (PD). The TIA features input/output DC-offset cancellation and is equipped with various analog control pins (NoXing, Vxing, Vmod and BW) which allow for zero-crossing adjustment, gain and peaking control.

Features

- 0.25 µm SiGe-BiCMOS technolgy
- Supports data rates of up to 56 Gbit/s
- Low power consumption: typ. 250mW
- Differential Output 100 Ω
- 3.3V power supply
- Small dimensions 1040 µm x 640 µm

Applications

- CEI-56G
- Fiber optics systems tests
- Research and development

Parameter	Typical (PD chips)	Notes
Data rate	Up to 56 Gbit/s	
Supply Voltage (V_{CC})	3.3 V	
Power dissipation	250 mW	
Differential output resistance	100 Ω	
Ambient Operating Temperature	-5 to +85°C	

Simplified Block Diagram

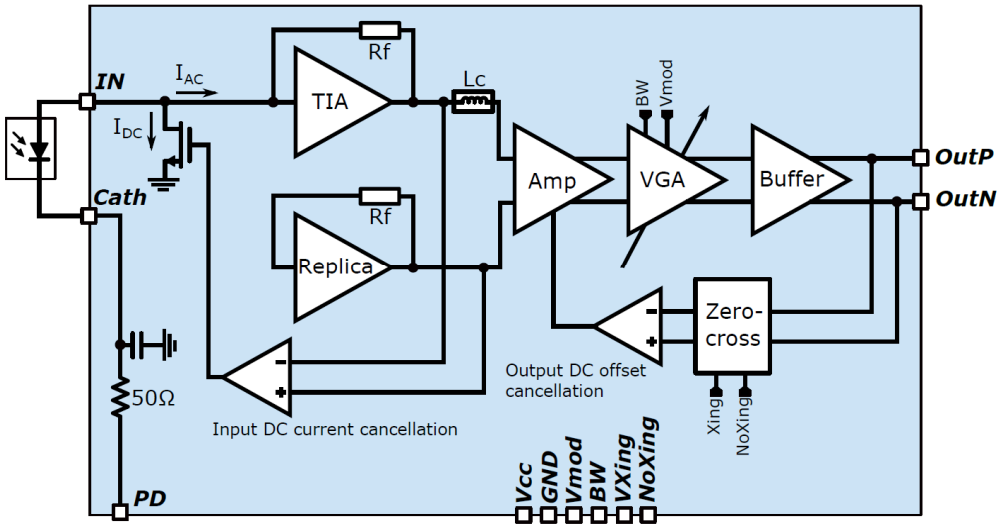


Figure 1. Simplified block diagram of the IC

The block diagram of the T56-250 is shown in Figure 1. It consists of four stages: an input transimpedance stage (TIA), a post-amplifier a variable gain amplifier (VGA) and a 50Ω output buffer. Series peaking with Lc between the first and second stage is used to increase the bandwidth. The IC has single-ended input (IN) and differential output (OutP OutN). A replica TIA provides the post-amplifier with DC-balanced inputs. A bias path for the photodiode is provided on-chip through the pin (PD) and cathode (Cath) that includes a low pass filter in order to damp eventual oscillations. The IC is operated from a single 3.3 V supply (VCC and GND) and is equipped with various analog control pins (Vmod, BW, NoXing, Vxing). Vmod defines the gain of the VGA. BW controls the frequency domain peaking. NoXing and VXing enable and control, respectively, the zero-crossing of the output signal.

Datasheet

T56-250v1

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Pad Layout

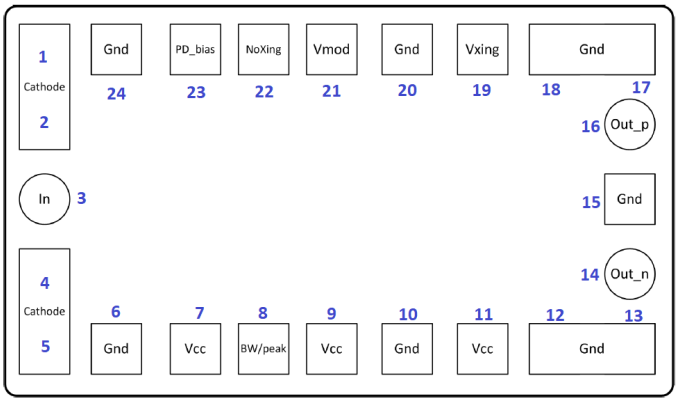

Figure 2. Pad layout of the IC

Pad description

Name	Pin	Symbol	Description	Function
In	3	IN	Input current (to PD anode)	
Out_p	16	OutP	HF output voltage (positive)	
Out_n	14	OutN	HF output voltage (negative)	
Vcc	7,9,11	Vcc	Supply voltage	
GND	6,10,12,13,15,17,18,20,24	GND	Ground	
PD_bias	23	PD	Photodiode bias	
Vmod	21	Vmod	VGA gain control	
BW/Peak	8	BW/Peak	Peaking control	
Vxing	19	Vxing	Zero-crossing control	
NoXing	22	NoXing	Xing control enable	
Cathode	1,2,4,5	Cath	Photodiode cathode	

Control Voltages Description

Vcc
Power supply of the IC.

PD_bias
Control voltage PD defines the reverse bias of the photodiode. This voltage is applied through an on-chip bias path that serves to damp eventual oscillations caused by the packaging parasitics.

Cathode
Photodiode cathode.

Vmod
Control voltage Vmod defines the VGA gain. It can be tuned between 1.2V (low gain setting) and 3.3V (high-gain setting), providing ~20dB gain control range. Differential S21 parameter change with Vmod is displayed in Fig. 3.

Vxing
Control voltage Vxing, tuned between 0.5V and 3.3V defines the position of the signal crossing point.

NoXing
Enables Xing control: if NoXing is connected to GND, Vxing has no effect and the zero crossing is automatically adjusted with the on-chip DC-cancellation loop. If NoXing is left open, zero-crossing adjustment through Vxing is enabled.

BW/Peak
Control voltage V_{bw} defines the use of capacitive bandwidth extension. Differential transimpedance gain (with PD model) with and without V_{bw} control is displayed on Fig. 5.
If this pin is left floating, the voltage is set to the typical value (0 V).

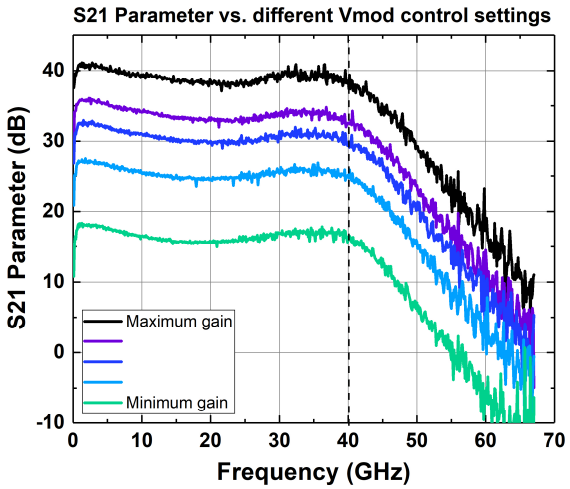

Figure 3. Influence of the Vmod control voltage on the S21 parameter

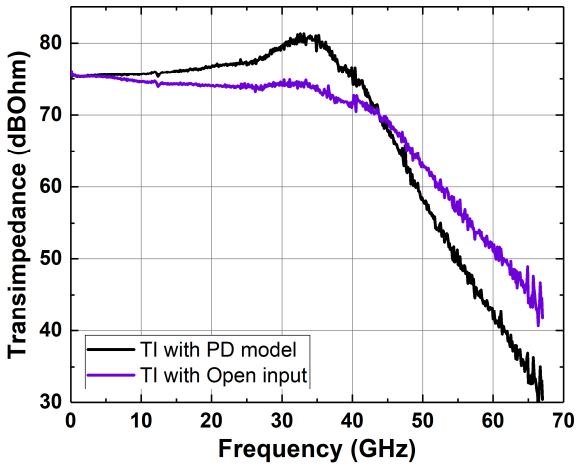

Figure 4. Measured differential transimpedance gain taking into effect the load characteristics.

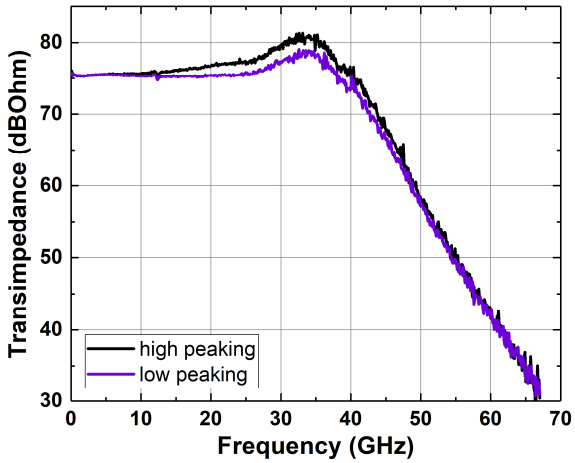

Figure 5. Differential transimpedance gain with and without Vbw peaking control.

Turn on conditions

To properly switch on the IC, apply Vcc;
Vmod, BW and Vxing can be applied simultaneously with or later than Vcc.

Operating conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input current (DC)			0.2		2	mApp
Input current (AC)			0		1.2	mA
Supply voltage	V_{cc}			3.3		V
VGA gain control	V_{mod}		1.2		3.3	V
Zero crossing adjustment	V_{xing}		0.5	-	3.3	V
Peaking control	V_{bw}	0		-	3.3	V
NoXing	V_{noxing}			GND		V
Photodiode bias	PD			5	5	V
Bondwire inductance for signal pins				250	400	pH
Bondwire inductance for cathode		multiple		4 x 250	4 x 400	pH

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features ESD protection, devices subjected to ESD stress may lose in performance and functionality.

Quality of the input signals should be monitored and supplied based on test circuit (Fig …)

Test circuit

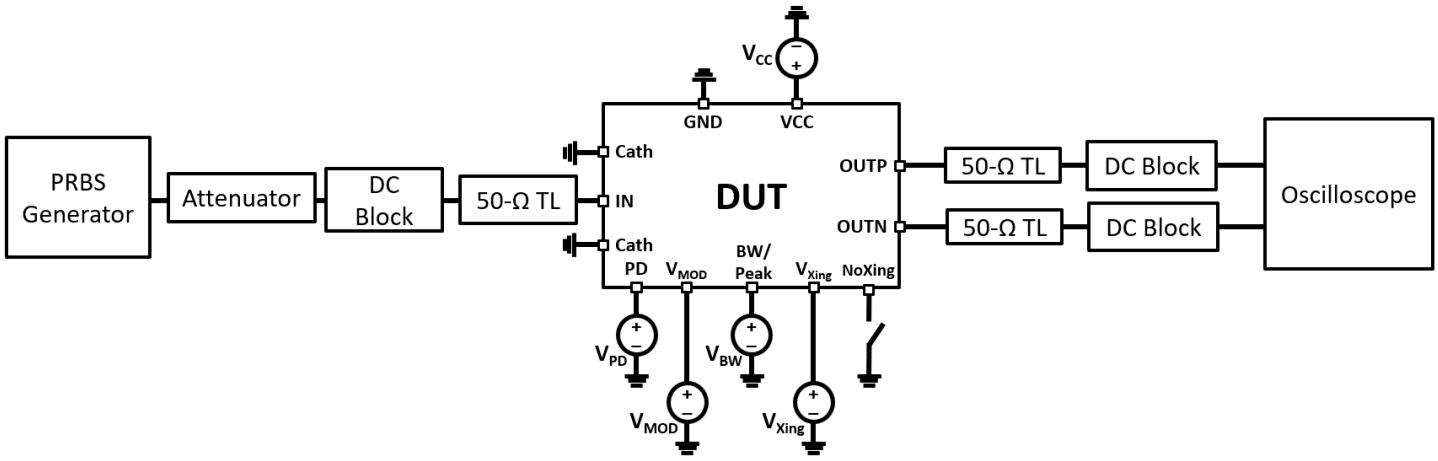

Figure 6. Test circuit

The functionality of the IC can be monitored and operated based on test circuit (Fig. 6)
300 pF external capacitor recommended to clean the Vcc DC signal.

Datasheet

T56-250v1

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Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input current (DC)			0.2		2.5	mApp
Input current (AC)					1.5	mA
Power supply voltage	V_{cc}	w/ respect to GND	-0.5		3.5	V
BW Vvga, Vmod	V_{bw} V_{xing}, V_{mod}	w/ respect to GND	0		3.5	V
Soldering temp		<10 sec			+300	°C
Operating temperature	T_{OP}		-5		+85	°C
Vcontrol currents (Vxing, VBW, Vmod)					2	mA

Characteristics & output parameters

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Data Rate				50	56	Gb/s
Differential output voltage				1		Vpp
Differential transimpedance gain			700		5800	Ω
S21 Bandwidth*				40		GHz
|S22|Output return loss		< 40GHz	12		5	dB
Input referred integrated noise**		45 GHz		14.2		pA/sqrt(Hz)
Rise/Fall time		20-80%		7/5		
Power dissipation				250		mW

* The bandwidth is stated for a 50 Ω load. The bandwidth is higher with a photo-diode, see Fig. 4.
** Integrated output noise was measured with the TIA in open input using the histogram function of the oscilloscope. Integrated input referred current noise was subsequently calculated as following (0.65mVrms is the noise of the oscilloscope module itself)

- $I_{n,in} = \frac{\sqrt{(8.3mV)^2-(0.65mV)^2}}{2900} = 2.85\ \mu A_{rms}$
- $I_{n,in,avg} = \frac{I_{n,in}}{\sqrt{40\ GHz}} = 14.2\ pA/\sqrt{Hz}$

All product specifications and descriptions are subject to change without notice.

Performance

Electrical measurements were performed on a 50 Ω load. Improvement of the electrical characteristics is expected in assembly with a photo-diode chip. The performance of the assembly strongly depends on the model of the optoelectronic device and assembly scheme.

Eye diagram at 56 Gbit/s (electrical)

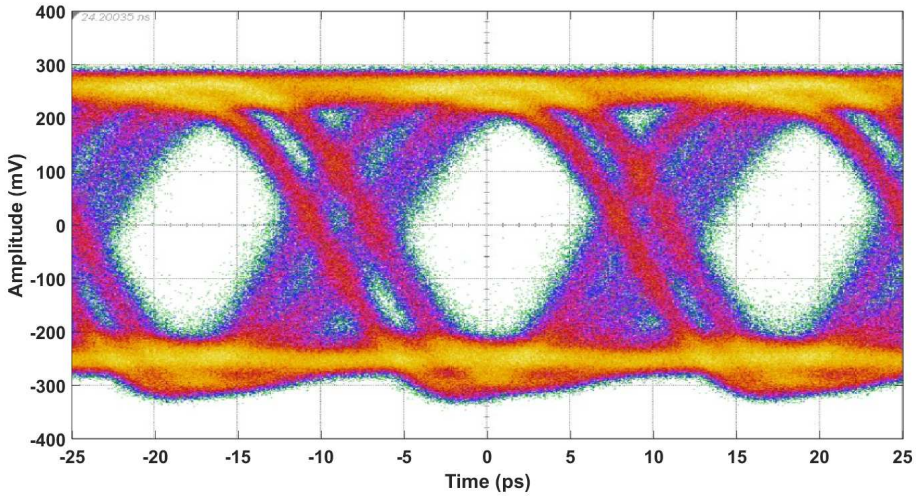

Figure 7Single-ended electrical eye-diagram at 56 Gbit/s bit rate.
max. BW, @ max. gain. @NoXing = GND, single-ended, 54mVpp at input.

S-Parameters

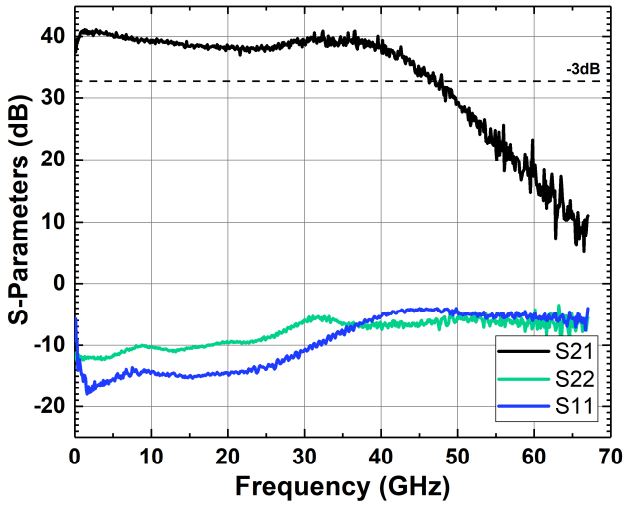

Figure 8. S21, S22 and S11 parameters measured on the IC

Datasheet

T56-250v1

Vertically Integrated Systems

Mechanical dimensions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Die width	W			1.04		mm
Die length	L			0.64		mm
Die thickness	H			200		µm
DC square pad dimensions				80		µm
RF octagonal pad dimensions				60		µm
Pad pitch				100		µm

Limited Qualification Notification

The T56-250Cv1 has been tested to meet specifications outlined in this data sheet at room temperature. However, it has not undergone full qualification testing or characterization and therefore may not meet the performance specifications over all extremes.

RoHS Compliant

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