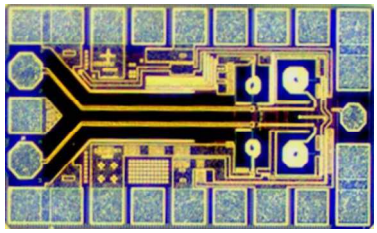
Datasheet

A56-230 VCSEL Driver

Vertically Integrated Systems

VCSEL driver
56 Gbit/s NRZ



Sample image only. Actual product may vary

Product Code: A56-230

Preliminary

Product Description

The A56-230 is a high speed VCSEL driver IC designed for directly modulated VCSELs in fiber optic transmission systems.

The VCSEL driver IC is designed to directly modulate common-cathode VCSEL. The IC has differential input (Vin+, Vin-) and single-ended output to the VCSEL anode. A ground for the VCSEL common cathode is also provided by the IC. It is operated with a single 3.3 V supply typically dissipating less than 200 mW of DC power when no load (VCSEL) is connected at the output.
The driver is also equipped with various analog control pins (Vxing, Vmod, Vbias). The zero-crossing can be adjusted with the Vxing pin. The VCSEL modulation current is controlled by varying the bias current swing with the Vmod, and the VCSEL bias current is controlled by Vbias pin.

Features

· up to 56 Gbit/s Laser Diode Driver for VCSELs
· differential input 100 Ω
· low power consumption
· small footprint

Applications

· CEI-56G
· Fiber optics systems tests
· Research and development

Parameter	Typical	Notes
Data rate	Up to 56 Gbit/s	
Supply Voltage (V_{DD})	3.3 V	
Power dissipation	200 mW	
Differential Input Resistance	100 Ω	
Ambient Operating Temperature	-5 to +85°C	

Simplified Block Diagram

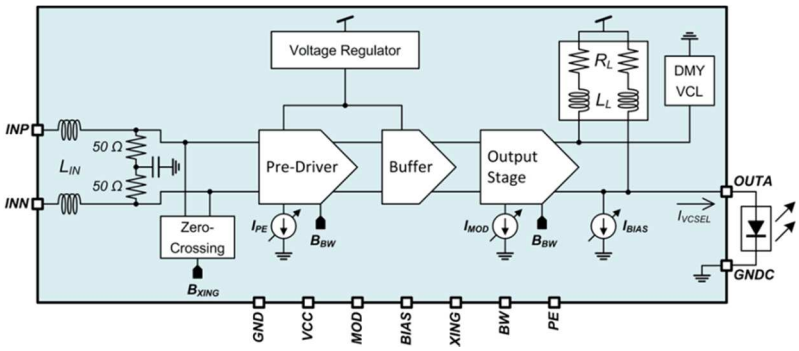


Figure 1. Simplified block diagram of the IC

The VCSEL driver IC is designed to directly modulate common-cathode VCSEL. The IC has differential input (INP, INN) and single-ended output (OUTA) to the VCSEL anode. A ground for the VCSEL common cathode (GNDC) is also provided by the IC. It is operated with a single 3.3 V supply (VCC and GND) and equipped with various analog control pins (MOD, BIAS, XING, BW, PE).

Pad Layout

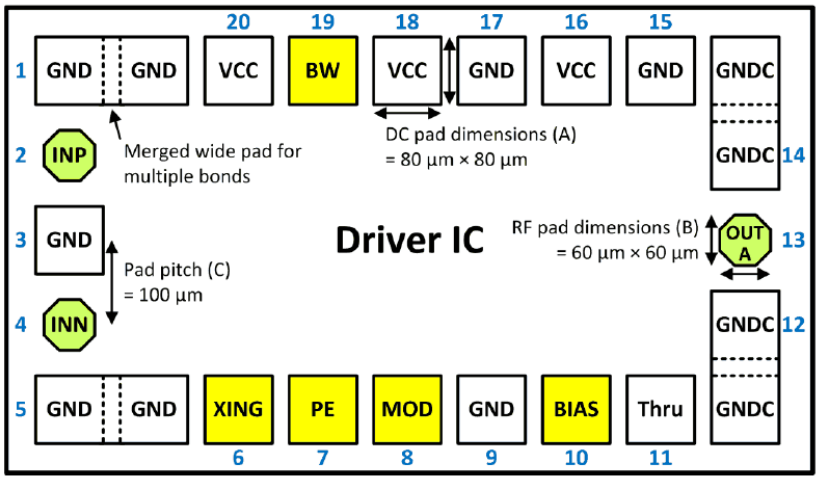


Figure 2. Pad layout of the IC

Pad description

Name	Pin	Symbol	Description	Function
In+	2	INP	HF input (positive)	HF Input
In -	4	INN	HF input (negative)	HF Input
Vcc	16,18,20	VCC	3.3 V supply voltage.	Supply
V bias	10	BIAS	Control voltage of VCSEL bias current.	Input
V mod	8	MOD	Modulation current (I_{MOD}) control	Input
V bw	19	BW	Analog control voltage of capacitive bandwidth extension.	Input
V xing	6	XING	Zero crossing control voltage	Input
V pe	7	PE	Analog control voltage of pre-emphasis level.	Input
V thru	11	Thru	Internal supply voltage monitoring.	Input
GND	1, 3, 5, 9, 15, 17	GND	Ground (0 V)	Ground
VCSEL cathode	12,14	GNDC	Ground to VCSEL cathode.	Output
VCSEL anode	13	OUTA	Output to VCSEL anode.	Output

Control Voltages Description

Vcc
Power supply of the IC.

Vbias
Control voltage V_{bias} defines the bias current provided to the VCSEL. The values expected at different V_{mod} voltages are displayed on Fig. 3. (simulated with a VCSEL model)

V_{mod}
Control voltage Vmod defines the modulation current (I_{mod}) provided to the VCSEL. The values expected at different V_{bias} voltages are displayed on Fig. 4 (simulated with a VCSEL model)

Vbw
Control voltage V_{bw} defines the use of capacitive bandwidth extension. Differential S21 parameter with and without V_{bw} control is displayed on Fig. 5 (measurement).
If this pin is left floating, the voltage is set to the typical value (0 V).

Vxing
Control voltage Vxing defines the position of the signal crossing point. If this pin is left floating, the voltage is set to the typical value (2.0 V).

V_{pe}
Control voltage V_{pe} defines the level of the pre-emphasis. If this pin is left floating, the voltage is set to the typical value (1.2 V).

V_{thru}
Control voltage V_{thru} is used for internal supply voltage monitoring.

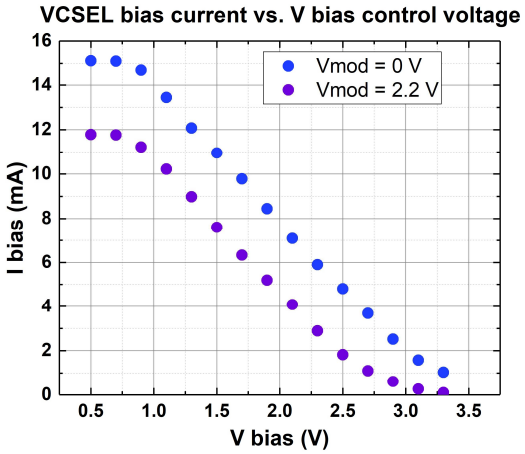


Figure 3. VCSEL bias current controlled by Vbias

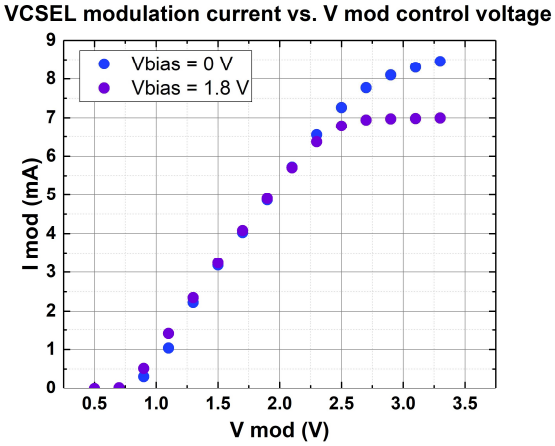


Figure 4. VCSEL modulation current controlled by Vmod

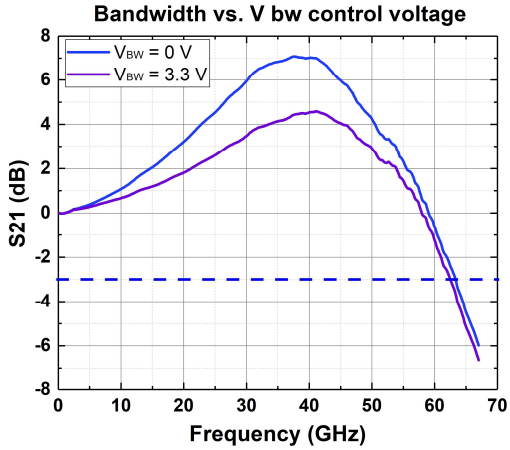


Figure 5. Measured Bandwidth controlled by Vbw

Turn on conditions

Before Vcc is applied, provide a proper Vbias first in order to ensure that too much bias current, higher than the absolute maximum current of a VCSEL, is not supplied. If Vcc is applied with the floating Vbias, the maximum bias current is supplied to the VCSEL. Other control voltages can be applied simultaneously with or later than Vcc.

Operating conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply voltage	V_{cc}			3.3	3.4	V
Bias current control	V_{bias}		0.7	1.8	3.3	V
Modulation current control	V_{mod}			2.2	3.3	V
Crossing control	V_{xing}			2.0	3.0	V
Peaking control voltage	V_{bw}			0	3.3	V
Pre-emphasis control voltage	V_{pe}			1.2	3.3	V
Bondwire inductance for signal pins				250	400	pH
Bondwire inductance for HF pins				62.5	100	pH
Bondwire length for signal pins				0.25	0.4	mm
Bondwire length for HF pins		multiple		4 x 62.5	4 x 100	um

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features ESD protection, devices subjected to ESD stress may lose in performance and functionality.

Test circuit

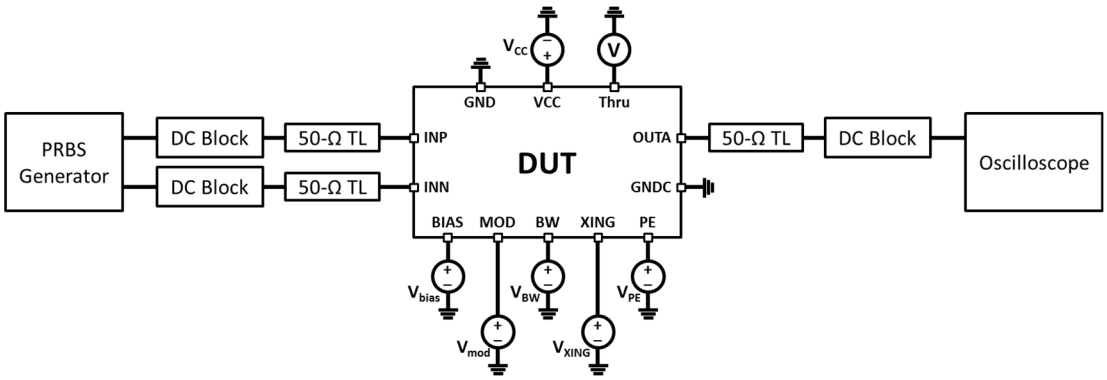


Figure 6. Test circuit

The functionality of the IC can be monitored and operated based on test circuit (Fig 6)

300 pF external capacitor recommended to clean the Vcc DC signal.

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Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	V_{cc}	w/ respect to GND	0		3.4	V
Vxing, Vmod, Vbias	V_{bias} V_{xing} V_{mod}	w/ respect to GND	0		3.3	V
Differential Input	V_{in+} V_{in-}	V_{in+} to V_{in-}	0.4	0.6	1.0	V
Operating Temperature	T_{OP}		-5		+85	°C
Vcontrol current limits					2	mA

Characteristics & output parameters

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Maximum data rate				56		Gbit/s
Bias current provided to VCSEL(sim)	I_{BIAS}		0	6	15	mA
Output modulation current provided to VCSEL (sim)	I_{MOD}		0	6	8	mA
S21 small-signal bandwidth		50Ω load		63		GHz
|S11| input return loss		<40 GHz	15		7	dB
Rise / Fall time (sim)	t_R / t_F	(20-80%)		6.5/7		ps
Max. deterministic jitter	J_D	rms		0.7		ps
Crosspoint Adjust (CPA) Range			40	50	65	%
Supply current consumption	I_{CC}		50	60		mA
Power consumption			165	200	230	mW

Simulated values are marked with (sim)

Performance

Electrical measurements were performed on a 50 Ω load. Improvement of the electrical characteristics is expected in assembly with a VCSEL chip. The performance of the assembly strongly depends on the model of the optoelectronic device and assembly scheme.

Eye diagram at 56 Gbit/s

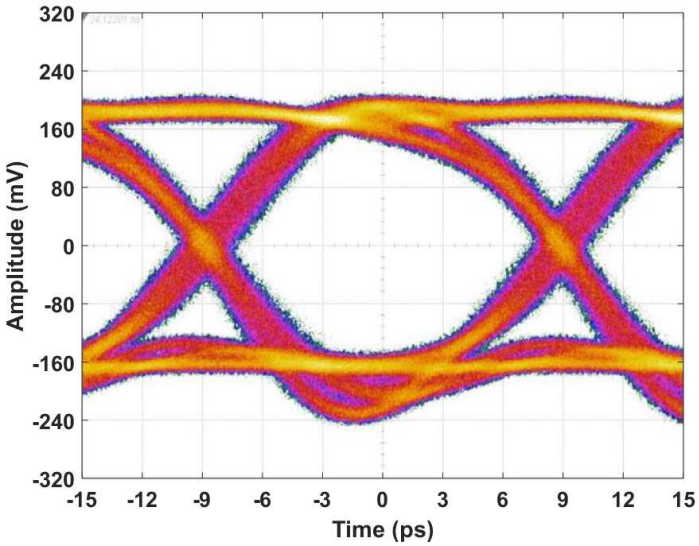

Figure 7. Electrical eye-diagram at 56 Gbit/s bit rate.
Driving conditions: Vbias = 1.8 V, Vmod = 3.0 V, Vbw = 3.3 V

S-Parameters (measurement)

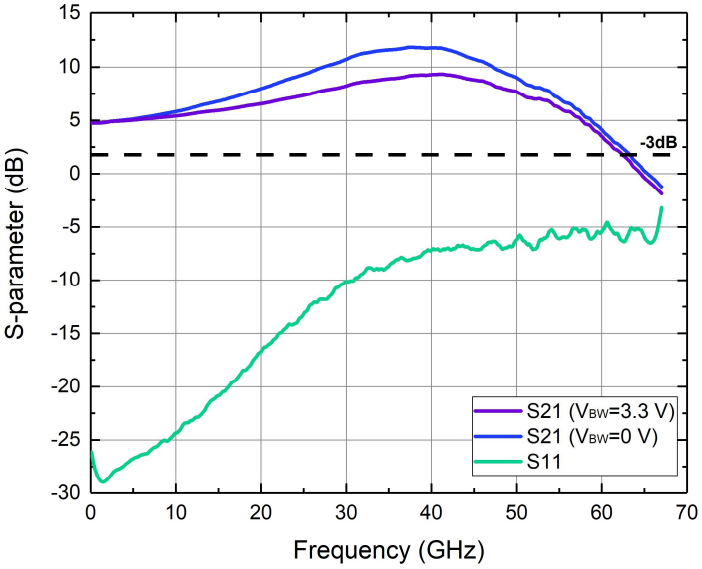

Figure 8. S21 and S11 parameters measured on the IC

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Mechanical dimensions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Die width	W			0.64		mm
Die length	L			1.04		mm
Die thickness	H			200		µm
DC square pad dimensions				80		µm
RF octagonal pad dimensions				60		µm
Pad pitch				100		µm

Limited Qualification Notification

The A56-230C has been tested to meet specifications outlined in this data sheet at room temperature. However, it has not undergone full qualification testing or characterization and therefore may not meet the performance specifications over all extremes.

RoHS Compliant

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